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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,592	07/25/2003	Takeshi Matsunaga	240900US2S	9746

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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,592	MATSUNAGA ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeh et al. (U.S. Patent No. 6,294,834). With regard to Claim 1, Yeh discloses on figure 1 a semiconductor device, comprising: a multilayer wiring structure including a plurality of wiring layers formed on a substrate (10), a capacitor (32) arranged in a predetermined wiring layer in the multilayer wiring structure and including a lower electrode (34), a dielectric film (36), and an upper electrode (38), a first via formed in the predetermined wiring layer and connected to a top surface of the upper electrode (38) of the capacitor, and a second via formed in an overlying wiring layer stacked on the predetermined wiring layer, the second via formed on the first via and the second via being connected to a wiring formed in the overlying wiring layer. For the purpose of further illustrating the teachings of Yeh, figure 1 is reproduced herein.

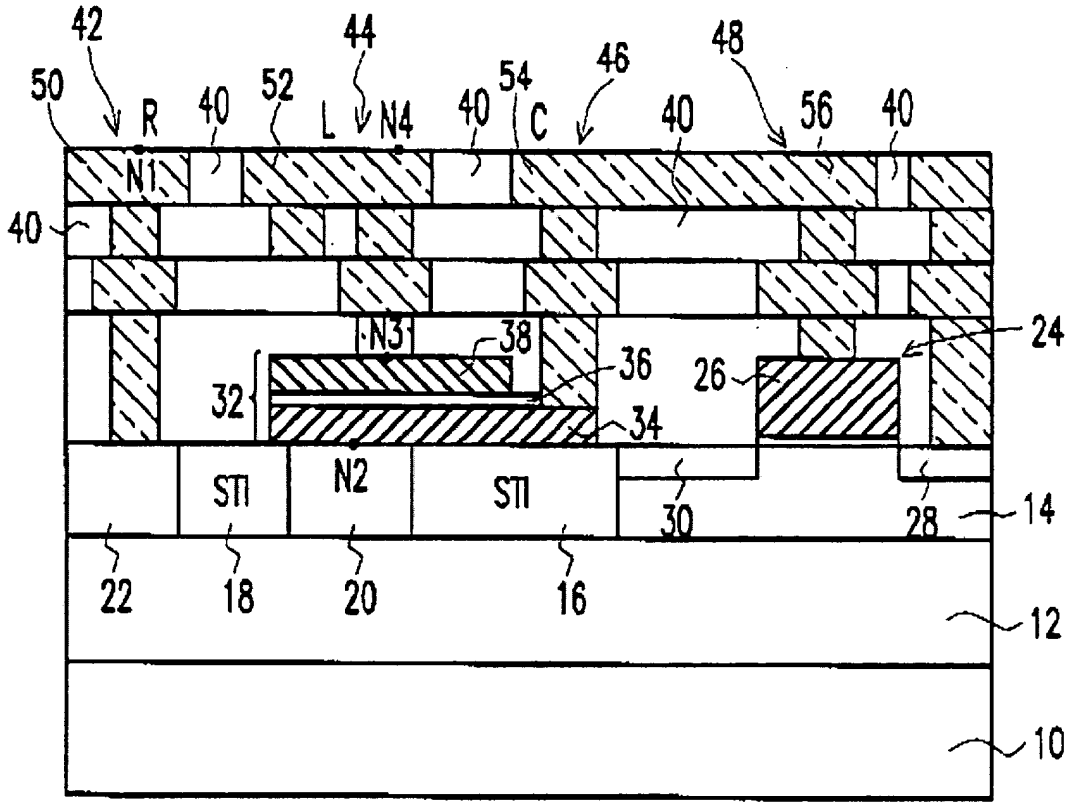

FIG. 1

With regard to Claim 3, Yeh discloses that the predetermined wiring layer has a third via formed on the lower electrode (34) and a wiring connected the third via and buried in a surface of the predetermined wiring layer. See figure 1.

With regard to Claim 7, Yeh discloses that the overlying wiring layer has a wiring connected to a top of the second via and buried in a surface of the overlying wiring layer. See figure 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 4, 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (U.S. Patent No. 6,294,834) in view of Moise (U.S. Patent No. 6,734,477). With regard to Claim 2, Yeh essentially discloses the claimed invention but fails to disclose the claimed first via having a larger cross area than that the second via. However, Moise discloses on figure 1 a semiconductor structure including a capacitor (50) arranged in a predetermined wiring layer (16) in a multilayer wiring structure and having a lower electrode (60), a dielectric film (62), and an upper electrode (64), a first via formed in the wiring layer (16) and connected to a top surface of the upper electrode (64) of the capacitor (50 or 52); and a second via formed in an overlying wiring layer (18) stacked on the wiring layer (16), wherein the second via is connected to the first via and has a cross-section larger than the first via. For the purpose of further illustrating the teachings of Moise, figure 1 is reproduced herein.

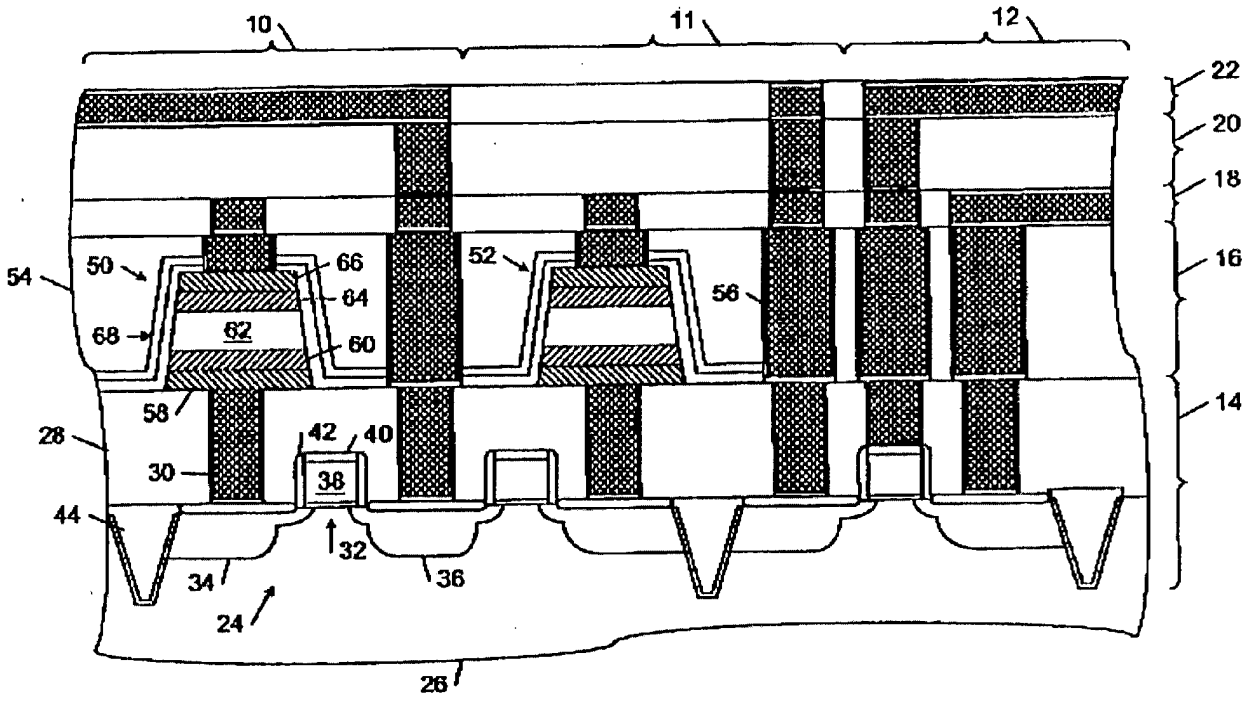

FIG. 1

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Yeh to include the claimed first via having a larger cross area than that the second via, as suggested by Moise, in order to reduce misalignment between the capacitor contact and contacts contained in upper wiring layers.

With regard to Claim 4, Yeh discloses that the predetermined wiring layer has a third via formed on the lower electrode (34) and a wiring connected the third via and buried in a surface of the predetermined wiring layer. See figure 1.

With regard to Claim 8, Yeh discloses that the overlying wiring layer has a wiring connected to a top of the second via and buried in a surface of the overlying wiring layer. See figure 1 which disclose the claimed arrangement.

With regard to Claims 9 and 10, Yeh discloses a third via formed on the lower electrode (34) of the capacitor is provided in the predetermined wiring layer, a fourth via formed connected to a top of the third via and provided in an overlying wired layer and the second and fourth vias are connected to the first and second wirings, respectively, buried in a surface of the overlying layer. See figure 1 which disclose the claimed arrangement.

Yeh fails to disclose the claimed fourth via being thinner than the third via. However, Moise discloses on figure 1 a semiconductor structure including a capacitor (50) arranged in a predetermined wiring layer (16) in a multilayer wiring structure and having a lower electrode (60), a dielectric film (62), and an upper electrode (64), a first via formed in the wiring layer (16) and connected to a top surface of the upper electrode (64) of the capacitor (50 or 52); and a second via formed in an overlying wiring layer (18) stacked on the wiring layer (16), wherein the second via is connected to the first via and has a cross-section larger than the first via. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Yeh to include the claimed fourth via being thinner than the third via, as suggested by Moise, in order to reduce misalignment between the capacitor contact and contacts contained in upper wiring layers.

With regard to Claims 11 and 12, a further difference between the claimed invention and Yeh is the claimed wiring buried in a surface of an underlying wiring layer and connected to the lower electrode of the capacitor. However, Moise discloses on figure 1 a capacitor (50) arranged in a predetermined wiring layer (16) in a multilayer wiring structure and having a lower electrode (60), a dielectric film (62), and an upper electrode (64), wherein the lower electrode (60) is connected to a wiring (30) buried in an underlying wiring layer (14). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Yeh to include the claimed wiring buried in a surface of an underlying wiring layer and connected to the lower electrode of the capacitor, as suggested by Moise, in order to form a contact to the source/drain regions and gate structures (column 4, lines 42-44).

With regard to Claim 13, Yeh discloses on figure 1 a semiconductor device, comprising: at least one impurity diffusion layer (28 or 30) formed in a first area of a semiconductor substrate (10), a plurality of wiring layers stacked on the semiconductor substrate (10) and including a first wiring layer having a contact connected to the impurity diffusion layer and a first wiring buried in the first wiring layer and connected to the contact, as can be seen on the right portion of the figure which clearly shows a wiring connected and contacting to the impurity diffusion region (28), a capacitor formed in a predetermined one of the plurality of wiring layers which predetermined wiring layer is formed on a second area different from the first area of the semiconductor substrate (10), the capacitor having a stacked structure of a lower electrode (34), a dielectric film (36), and an upper electrode (38), a first via formed on at least the upper electrode (38) formed in the predetermined wiring layer, an upper wiring layer having an interlayer insulating film (40)

stacked on the predetermined wiring layer, a second via formed in the interlayer insulating film, connected to the first via and a second wiring connected to the second via and buried in a surface portion of the upper wiring layer.

Yeh fails to disclose the claimed second via being thinner than the first via. However, Moise discloses on figure 1 a semiconductor structure including a capacitor (50) arranged in a predetermined wiring layer (16) in a multilayer wiring structure and having a lower electrode (60), a dielectric film (62), and an upper electrode (64), a first via formed in the wiring layer (16) and connected to a top surface of the upper electrode (64) of the capacitor (50 or 52); and a second via formed in an overlying wiring layer (18) stacked on the wiring layer (16), wherein the second via is connected to the first via and has a cross-section larger than the first via. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Yeh to include the claimed fourth via being thinner than the third via, as suggested by Moise, in order to reduce misalignment between the capacitor contact and contacts contained in upper wiring layers.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (U.S. Patent No. 6,294,834) in view of Jain et al. (U.S. Patent No. 6,417,092). With regard to Claims 5 and 6, Yeh essentially discloses the claimed invention but fail to disclose the claimed copper diffusion stopper film formed on the surface of the predetermined wiring layer. However, Jain discloses a semiconductor device including a first metal layer with devices (10), metal contacts (12), copper conductor (14) and a layer (15), which serves as a barrier against diffusion of copper

between metal levels. See column 4, lines 10-17 and figure 2b. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Yeh to include discloses the claimed invention but fail to disclose the claimed copper diffusion stopper film formed on the surface of the predetermined wiring layer, as suggested by Jain, in order to provide a layer which prevents copper diffusion and can also serve as an etch-stop with a range of insulating materials. See column 4, lines 10-17 and lines 28-36.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (U.S. Patent No. 6,294,834) in view of Moise (U.S. Patent No. 6,734,477) and further in view of Jain et al. (U.S. Patent No. 6,417,092). With regard to Claims 5 and 6, Yeh and Moise essentially disclose the claimed invention but fail to disclose the claimed copper diffusion stopper film formed on the surface of the predetermined wiring layer. However, Jain discloses a semiconductor device including a first metal layer with devices (10), metal contacts (12), copper conductor (14) and a layer (15), which serves as a barrier against diffusion of copper between metal levels. See column 4, lines 10-17 and figure 2b. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Yeh and Moise to include discloses the claimed invention but fail to disclose the claimed copper diffusion stopper film formed on the surface of the predetermined wiring layer, as suggested by Jain, in order to provide a layer which prevents copper diffusion and can also serve as an etch-stop with a range of insulating materials. See column 4, lines 10-17 and lines 28-36.

Response to Arguments

5. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
6/12/05

TOM THOMAS
SUPERVISORY PATENT EXAMINER